Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims

1. (currently amended) Digital signal processing (DSP) circuitry that independently processes a plurality of multi-channel data signals, comprising:

a plurality of columns of registers, each said column comprising an input and a plurality of registers arranged in serial; and

interconnection circuitry for allowing successive channels of said plurality of multi-channel data signals to be selectively shifted through said plurality of registers in each said column and to also be selectively shifted through a plurality of registers in at least one other of said plurality of columns, wherein said interconnection circuitry allows a value at the input of each column to be selectively routed to any said register in said respective column by bypassing any register or registers that precede said register in said respective column.

2. (previously presented) The circuitry of claim 1, further comprising utilization circuitry for operating on a first piece of data output by a register in a first of said columns and a second piece of data output by a register in a second of said columns, wherein the first and second pieces of

data each corresponds to a first channel of the plurality of multi-channel data signals.

3.   (original) The circuitry of claim 2, wherein said utilization circuitry comprises circuitry selected from the group consisting of adder circuitries, multiplier circuitries, and a combination thereof.

4.   (original) The circuitry of claim 1, wherein the interconnection circuitry comprises:

a multiplexer circuit associated with each register in each said column.

5.   (original) The circuitry of claim 1, wherein said interconnection circuitry allows successive data signals to be shifted to as many different said plurality of columns as needed such that the output of each of those columns is used as an input to a finite impulse response filter function.

6.   (previously presented) The circuitry of claim 5, wherein a respective register in each of those columns provides a respective piece of the output data used as the input to the filter function, wherein each respective piece of the output data corresponds to a first channel of the plurality of multi-channel data signals.

7.   (original) The circuitry of claim 1, wherein said interconnection circuitry can selectively route data signals past one or more of said registers in each said column.

8.   (previously presented) The circuitry of claim 1 wherein said circuitry is mounted on a programmable logic device.

9.   (original) The programmable logic device defined in claim 8 further comprising:

routing circuitry for selectively supplying signals to and receiving signals from the DSP circuitry.

10.   (original) The programmable logic device defined in claim 9 further comprising:

programmable logic circuitry connected to the routing circuitry.

11.   (original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 8 coupled to the processing circuitry and the memory.

12.   (previously presented) The circuitry of claim 8 wherein said circuitry is mounted on a printed circuit board.

13. (original) The printed circuit board defined in claim 12 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

14. (original) The printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

15. (currently amended) A programmable logic device (PLD), comprising:

digital signal processing (DSP) circuitry that supports multiple channels of data being transmitted on the same carrier, said DSP circuitry comprising:

tap delay line circuitry that comprises registers for registering the data of each of the multiple channels such that the data of each channel is not mixed with the data of any other channel, wherein the tap delay line circuitry comprises:

an input; and

interconnection circuitry that allows a value received at the input to be selectively routed to any register of said registers in said tap delay line circuitry by bypassing any register or registers that precede said register in said tap delay line circuitry; and

utilization circuitry that performs a function on data received from said tap delay line circuitry.

16. (original) The PLD of claim 15, wherein said tap delay line circuitry comprises:

at least two columns of registers, each column including at least two registers arranged in serial;

a multiplexer circuit respectively associated with a register of each said column, said multiplexer circuit operative to select one of at least two input signals being applied to said multiplexer circuit for application to said associated register, one of said input signals being one of said plurality of multi-channel signals, and another one of said input signals being the output signal of a register that is conveyed by a tap delay line from a register in a column different than the column said multiplexer circuit applies said input signal to.

17. (original) The DSP circuitry of claim 16, wherein said associated register is a leading register in each said column.

18. (original) The DSP circuitry of claim 16, wherein the output signal of the register being conveyed by the tap delay line is the output of a trailing register in each said column.

19. (original) The DSP circuitry of claim 16, wherein the tap delay line conveys an output signal of a register that is being provided to a first tap to a multiplexer

circuit associated with a column that provides an output signal to a second tap.

20. (original) The DSP circuitry of claim 15, wherein said utilization circuitry selectively operates on signals output by a register in each said column.

21. (original) The DSP circuitry of claim 16, further comprising bypass circuitry for enabling the selected input signal to be routed directly to one of said at least two registers in said column of registers.